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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,060	03/19/2004	Takayuki Kondo	118944	8241

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EXAMINER	
KESHAVAN, BELUR V	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/804,060	KONDO, TAKAYUKI	
	Examiner	Art Unit	
	Belur V. Keshavan	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/28/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo (US Pub. No.: 2004/0036078) in view of Feng et al. (US Pub. No.: 2005/0040432).

Regarding claims 1-4, 8, 9 and 13, Kondo discloses on paragraphs [0130] and [0154] and in figure 15 an HBT transistor (113) comprising an insulating substrate (171); a first metal film functioning as a collector wiring formed on a bottom surface of a first layer, a second metal film functioning as base wiring formed in an area other than the area where the third layer is formed on the second layer and a third metal film functioning as emitter wiring formed on the top of the third layer and all three metal layers collectively represented as (191) and disposed on the insulating substrate without intersecting one another but contacting the collector, base and emitter of a transistor formed by laminating a plurality of

semiconductor layers (paragraph [0086]). Kondo lacks the details of semiconductor layers. Feng discloses a transistor in figure 12 comprising a N-type semiconductor as the first layer (190) being as a collector, a P-type semiconductor as the second layer (140) covering the first layer completely being as a base and N-type semiconductor as the third layer on the second layer being as a emitter. It would have been obvious to one of ordinary skill in the art to use the teachings of Feng et al. to modify or add to the device described in Kondo.

Regarding claim 5, Feng discloses in figure 1, wherein the first layer (130) and the second layer (140) are all formed in a rectangular plate shape and the third layer (150) being formed in a longer and narrower than that of the first and the second layer.

Regarding claim 6, Kondo discloses, in the figure 15, wherein the first layer, the second layer, and the third layer being formed so as to cross on a top surface of the first metal film.

Regarding claim 7, Kondo discloses, in the figure 1 and in paragraph [0086], wherein the first, the second and the third layers are formed as tile-shaped elements.

Regarding claims 11 and 12, Kondo discloses in paragraph [0028] plurality of devices with three stacked layers for each device on the substrate but silent about the coupling all the second layers and all the third layers to second metal film and third metal film respectively. It would have been obvious to one of ordinary skill in the art to couple all the second layers and all the third layers to the second metal film and third metal film respectively for faster operation of the similar type of devices and to achieve higher density of the devices.

Regarding claim 14, Kondo discloses in figure 15 wherein a portion of the second metal film (191) that is not coupled to the second layer in the second metal film being directly provided on the insulating substrate (171), and a portion of the third metal film (191) that is not coupled to the third layer in the third metal film being directly provided on the insulating substrate.

Regarding claim 15, Kondo discloses, in paragraphs [0028] and [0041] and in claims 20, 21 and 22, an electronic device comprising an optical interconnection circuit having the HBT.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo (US Pub. No.: 2004/0036078) in view of Feng et al. (US Pub. No.: 2005/0040432) and further in view of Yanagisawa (US Pub. No.: 2003/0160266).

Regarding claim 10, Kondo in view of Feng teaches all of the features and limitations of the base claims but lack a HBT transistor using GaAs layers for collector and base regions and AlGaAs layer for emitter region. However, the HBT transistor using GaAs layers for collector and base regions and AlGaAs layer for emitter is notoriously well known in the art of which the examiner takes an Official Notice. In support of this assertion, the examiner cites Yanagisawa wherein Yanagisawa discloses, in paragraph [0081], a HBT device with GaAs layers as the collector and the base and AlGaAs layer as the emitter. It would have been obvious to one of ordinary skill in the art to use the teachings of Yanagisawa to modify or add to the device described in Kondo.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Belur V. Keshavan whose telephone number is 571-272-1894. The examiner can normally be reached on 8-4:30 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BVK. BVK
May 3, 2005.

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800